In the Specification:

Please amend the paragraph on page 4, line 10 to page 5, line 4 of the specification to read as follows:

> According to an exemplary embodiment of the present invention, there is provided a buffer including a first memory and a second memory, the second memory being less dense but faster than the first memory. At least one queue is associated with the first and second memories and serves as a pointer to point to the locations in the first and second memories where data packets are stored. Incoming data packets are initially stored in the first memory. Individual data packets are subsequently transferred from the first memory to the second memory upon the individual data packet becoming the head-of-line (HOL) packet, i.e., the packet appearing at the top of the at least one queue. By maintaining the head-of-line packets in the fast second memory while maintaining the remaining packets in the denser first memory, the buffer is advantageously capable of providing better performance in a relatively efficient manner.

Please amend the paragraph on page 6, lines 1-2 of the specification to read as follows:

Figure 2 is a ~~flow chart illustrating an operation of the packet buffer of Figure 1~~ block diagram of a system having the packet buffer of Figure 1 therein;

Please amend the paragraph on page 6, lines 3-4 of the specification to read as follows:

Figure 3 is a ~~block diagram of a system having the packet buffer of Figure 1~~ flow chart illustrating an operation of the packet buffer of Figure 1; and

Please amend the paragraph on page 15, line 9 to page 16, line 5 of the specification to read as follows:

In this example, a series of packets associated with a particular queue 9 is sequentially retrieved from packet buffer 1 for subsequent transmission to the predetermined destination node. Specifically, the address of the HOL packet is provided by the particular queue 9. With the address of the HOL packet, the HOL packet is retrieved from second memory 5 (SRAM) and placed on the data I/O for subsequent transmission to the destination node. The particular queue 9 is updated to point to the new HOL packet. In the event the particular queue 9 is not empty following it being updated, the address of the new HOL packet may be received and the packet retrieved from first memory 3 (drDRAM) and

placed in second memory 5 (SRAM). Further, the new address of the new HOL packet is placed in the particular queue 9 so that the particular queue is able to point to the correct location in second memory 5 where the new HOL packet is stored. At this point, packet buffer 1 is ready to provide another packet for subsequent transmission to a destination node.